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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/631,246	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/27/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-34 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 11/27/2007.

Maintained Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,973,562).

5. As per claim 9:

McGrath disclosed a method of decoding instructions from a first instruction set and a second instruction set, comprising:

Decoding instructions from the first instruction set in a first mode and decoding instructions from the second instruction set in a second mode, wherein the decoding of both instruction sets is performed on a separate decoders (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-45 and column 8 lines 63-67 continued to column 9 lines 1-27)(The first instruction set is the instructions that execute the 64-bit OS and the second instruction set is the instructions that execute the 32-bit application code. It's inherent that the instructions fetched from the instruction cache are decoded

before they are executed. Thus, it's obvious to one of ordinary skill in the art that decode logic is contained within element 14 to decode instructions from both instruction sets.);

Switching the decoding from one mode to another for one instruction (McGrath: Figure 10 element 142, column 15 lines 29-36)(The prefix field allows an override of the current operating mode for the current instruction. It allows for different operand and address sizes.);

Switching the decoding from one mode to another for a plurality of instructions (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set.).

Setting a status register that indicates whether the decode logic is decoding instructions in the first mode or the second mode (McGrath: Figure 1 elements 24a, 26, and 28, column 4 lines 49-67 continued to column 5 lines 1-20)(A plurality of status registers contain the bits that determine the operating mode of the execution core. It's obvious to one of ordinary skill in the art at the time of the invention that these control registers could be combined so that the bits indicating the operating mode are in a single register. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.).

6. As per claim 10:

McGrath disclosed the method of claim 9, wherein the step of switching the decoding from one mode to another for the one instruction comprises detecting a temporary instruction that indicates the one instruction belongs to another instruction set (McGrath: Figure 10 element 142, column 15 lines 29-36)(The prefix field allows an override of the current operating mode for the current instruction. It allows for different operand and address sizes. An instruction with different operand sizes is an instruction of a different instruction set, even if this is the only difference between the instruction sets.).

7. As per claim 11:

McGrath disclosed the method of claim 10, wherein the switching the decoding from one mode to another comprises switching from the first mode to the second mode for the one instruction, wherein the one instruction belongs to the second instruction set (McGrath: Figure 10 element 142, column 15 lines 29-36)(The prefix field allows an override of the current operating mode for the current instruction. It allows for different operand and address sizes. An instruction with different operand sizes is an instruction of a different instruction set, even if this is the only difference between the instruction sets.).

8. As per claim 12:

McGrath disclosed the method of claim 10, wherein the switching the decoding from one mode to another comprises switching from the second mode to the first mode for the one instruction, wherein the one instruction belongs to the first instruction set (McGrath: Figure 10 element 142, column 15 lines 29-36)(The prefix field allows an

override of the current operating mode for the current instruction. It allows for different operand and address sizes. An instruction with different operand sizes is an instruction of a different instruction set, even if this is the only difference between the instruction sets.).

9. As per claim 13:

McGrath disclosed the method of claim 10, wherein the first and second instruction sets each comprise the temporary instruction (McGrath: Figure 10 element 142, column 15 lines 29-36)(The prefix field allows an override of the current operating mode for the current instruction. It allows for different operand and address sizes. An instruction with different operand sizes is an instruction of a different instruction set, even if this is the only difference between the instruction sets. All instructions contain the prefix.).

10. As per claim 14:

McGrath disclosed the method of claim 9, wherein the switching the decoding from one mode to another for a plurality of instructions comprises detecting a temporary instruction that indicates the one instruction belongs to another instruction set (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set.).

11. As per claim 15-17:

Claims 15-17 essentially recite the same limitations of claim 6. Therefore, claims

15-17 are rejected for the same reasons as claim 6.

12. As per claim 18-20:

Claims 18-20 essentially recite the same limitations of claim 8. Therefore, claims 18-20 is rejected for the same reasons as claim 8.

13. Claims 1, 5-6, 8, and 21-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,973,562), in view of Tran (U.S. 6,367,006).

14. As per claim 1:

McGrath disclosed a processor, comprising:

Decode logic configured to decode instructions from a first instruction set in a first mode and configured to decode instructions from a second instruction set in a second mode (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-45 and column 8 lines 63-67 continued to column 9 lines 1-27)(The first instruction set is the instructions that execute the 64-bit OS and the second instruction set is the instructions that execute the 32-bit application code. It's inherent that the instructions fetched from the instruction cache are decoded before they are executed. Thus, it's obvious to one of ordinary skill in the art that decode logic is contained within element 14 to decode instructions from both instruction sets.), wherein the decode logic is configured to switch from one mode to another temporarily or for a plurality of instructions (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-29)(The execution core operates according to the operating mode. Figure 4 element 60 shows the instructions that switch between operating modes.);

A status register coupled to the decode logic and configured to indicate whether the decode logic is decoding instructions in the first more or the second mode (McGrath: Figure 1 elements 24a, 26, and 28, column 4 lines 49-67 continued to column 5 lines 1-20)(A plurality of status registers contain the bits that determine the operating mode of the execution core. It's obvious to one of ordinary skill in the art at the time of the invention that these control registers could be combined so that the bits indicating the operating mode are in a single register. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.).

Wherein the first and second instruction sets each comprise an instruction that temporarily switches the decode logic from one mode to another for at least one subsequent instruction (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set.).

McGrath failed to teach pre-decode logic coupled to the decode logic and configured to operate in parallel with the decode logic.

However, Tran disclosed pre-decode logic coupled to the decode logic and configured to operate in parallel with the decode logic (Tran: Figure 3 element 50, column 15 lines 4-19).

The advantage of using a predecoder is that branch instructions can be detected and if predicted to be taken, prefetching can occur faster than if using a normal decoder

(Tran: Column 15 lines 4-11). One of ordinary skill in the art would have been motivated by this advantage to implement a predecoder. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a predecoder for the advantage of quicker prefetching of instructions at the target address.

15. As per claim 5:

McGrath and Tran disclosed the processor of claim 1, wherein the first instruction set comprises an instruction that switches the decode logic from the first mode to the second mode for a plurality of instructions (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, and terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, and return from exception are instructions within the first instruction set that switch to the second instruction set. It's obvious to one of ordinary skill in the art that these call instructions would result in the called routine executing a plurality of instructions.).

16. As per claim 6:

McGrath and Tran disclosed the processor of claim 1, wherein the second instruction set comprises an instruction that switches the decode logic from the first mode to the second mode for a plurality of instructions (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, and terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, and return from exception are

instructions within the first instruction set that switch to the second instruction set. It's obvious to one of ordinary skill in the art that these call instructions would result in the called routine executing a plurality of instructions. The second instruction set is the first mode and the first instruction set is the second mode.).

17. As per claim 8:

McGrath and Tran disclosed the processor of claim 1, wherein the second instruction set comprises an instruction that switches the decode logic from the second mode to the first mode for a plurality of instructions (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, and terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, and return from exception are instructions within the first instruction set that switch to the second instruction set. It's obvious to one of ordinary skill in the art that these call instructions would result in the called routine executing a plurality of instructions.).

18. As per claim 21:

McGrath disclosed a processor, comprising:

Decode logic configured to decode instructions from a first instruction set in a first mode and configured to decode instructions from a second instruction set in a second mode (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-45 and column 8 lines 63-67 continued to column 9 lines 1-27)(The first instruction set is the instructions that execute the 64-bit OS and the second instruction set is the instructions that execute the 32-bit application code. It's inherent that the instructions fetched from

the instruction cache are decoded before they are executed. Thus, it's obvious to one of ordinary skill in the art that decode logic is contained within element 14 to decode instructions from both instruction sets.);

A status register configured to indicate whether the decode logic is decoding instructions in the first mode or second mode (McGrath: Figure 1 elements 24a, 26, and 28, column 4 lines 49-67 continued to column 5 lines 1-20)(A plurality of status registers contain the bits that determine the operating mode of the execution core. It's obvious to one of ordinary skill in the art at the time of the invention that these control registers could be combined so that the bits indicating the operating mode are in a single register. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.).

Wherein the first and second instruction sets each comprise the temporary instruction and wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set. These instructions are temporary and permanent instructions because they indicate subsequent instructions will be from another mode.).

McGrath failed to teach pre-decode logic coupled to the decode logic and configured to pre-decode instructions in parallel with the decode logic wherein the pre-

decode logic pre-decodes for a temporary instruction that switches the decode logic from one mode to another for a subsequent instruction.

However, Tran disclosed pre-decode logic coupled to the decode logic and configured to pre-decode instructions in parallel with the decode logic wherein the pre-decode logic pre-decodes for a temporary instruction that switches the decode logic from one mode to another for a subsequent instruction (Tran: Figure 3 element 50, column 15 lines 4-19)(The combination results in the predecoder detecting the switching instructions from both instruction sets.).

The advantage of using a predecoder is that branch instructions can be detected and if predicted to be taken, prefetching can occur faster than if using a normal decoder (Tran: Column 15 lines 4-11). One of ordinary skill in the art would have been motivated by this advantage to implement a predecoder. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a predecoder for the advantage of quicker prefetching of instructions at the target address.

19. As per claim 22:

McGrath and Tran disclosed the processor of claim 21, wherein the temporary instruction indicates that the subsequent instruction belongs to another instruction set and causes the decode logic to switch from one mode to another (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception

are instructions within the first instruction set that switch to the second instruction set. The instructions at the target address are from the other instruction set.).

20. As per claim 23:

McGrath and Tran disclosed the processor of claim 22 wherein the decode logic temporarily switch from the first mode to the second mode, and wherein the subsequent instruction belongs to the second instruction set (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-45 and column 8 lines 63-67 continued to column 9 lines 1-27)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set. It's obvious to one of ordinary skill in the art that these instructions change the mode in the status register to indicate that the mode is changing to the other instruction set.).

21. As per claim 24:

McGrath and Tran disclosed the processor of claim 22, wherein the decode logic temporarily switches from the second mode to the first mode, and wherein the subsequent instruction belongs to the first instruction set (McGrath: Figures 1 and 4 elements 14 and 60, column 4 lines 26-45 and column 8 lines 63-67 continued to column 9 lines 1-27)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set. It's obvious to one of ordinary skill in the art that these

instructions change the mode in the status register to indicate that the mode is changing to the other instruction set.).

22. As per claim 25:

McGrath and Tran disclosed the processor of claim 21, wherein the subsequent instruction is the first permanent instruction that switches the decode logic permanently from the first the mode to the second mode (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set. The instructions at the target address are from the other instruction set. It's obvious to one of ordinary skill in the art that the target address instruction could be an instruction that jumps back to the original instruction set.).

23. As per claim 26:

McGrath and Tran disclosed the processor of claim 21, wherein the second permanent instruction switches the decode logic from the second mode to the first mode for a plurality of instructions (McGrath: Figure 4 element 64, column 9 lines 62-67 continued to column 10 lines 1-24)(The call, exception, or terminate instructions are instructions within the second instruction set that switch to the first instruction set. The launch, return from call, or return from exception are instructions within the first instruction set that switch to the second instruction set. The instructions at the target address are from the other instruction set.).

24. As per claim 27:

Claim 27 essentially recites the same limitations of claim 21. Claim 27 additionally recites the following limitations:

A main processor coupled to a coprocessor (The coprocessor is the processor of McGrath. Official notice is given that another processor could be coupled to the processor of McGrath for the advantage of increased computing power for the processor.)

25. As per claim 28:

Claim 28 essentially recites the same limitations of claim 22. Therefore, claim 28 is rejected for the same reasons as claim 22.

26. As per claim 29:

Claim 29 essentially recites the same limitations of claim 23. Therefore, claim 29 is rejected for the same reasons as claim 23.

27. As per claim 30:

Claim 30 essentially recites the same limitations of claim 24. Therefore, claim 30 is rejected for the same reasons as claim 24.

28. As per claim 31:

Claim 31 essentially recites the same limitations of claim 25. Therefore, claim 31 is rejected for the same reasons as claim 25.

29. As per claim 32:

Claim 32 essentially recites the same limitations of claim 26. Therefore, claim 32 is rejected for the same reasons as claim 26.

30. As per claim 33:

McGrath and Tran disclosed the system of claim 27, wherein the system comprises a cellular telephone (Official notice is taken that the processing system could be part of a cellular telephone.).

31. Claims 2-4 and 7 are rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,973,562), in view of Tran (U.S. 6,367,006), further in view of Seal et al. (U.S. 6,965,984).

32. As per claim 2:

McGrath and Tran disclosed the processor of claim 1.

McGrath and Tran failed to teach wherein the first and second instruction sets each comprise a Java Impdep1 Bytecode that temporarily switches the decode logic from one mode to another.

However, Seal disclosed wherein the first and second instruction sets each comprises a Java Impdep1 Bytecode that temporarily switches the decode logic from one mode to another (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the

current combination of McGrath and Tran.

33. As per claim 3:

McGrath and Tran disclosed the processor of claim 1.

McGrath and Tran failed to teach wherein the first instruction set comprises a first reserved Java Bytecode that temporarily switches the decode logic from the first mode to the second mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the second instruction set.

However, Seal disclosed wherein the first instruction set comprises a first reserved Java Bytecode that temporarily switches the decode logic from the first mode to the second mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the second instruction set (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of McGrath and Tran.

34. As per claim 4:

McGrath and Tran disclosed the processor of claim 1.

McGrath and Tran failed to teach wherein the second instruction set comprises a second reserved Java Bytecode that temporarily switches the decode logic from the

second mode to the first mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the first instruction set.

However, Seal disclosed wherein the second instruction set comprises a second reserved Java Bytecode that temporarily switches the decode logic from the second mode to the first mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the first instruction set (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of McGrath and Tran.

35. As per claim 7:

McGrath, Tran, and Seal disclosed the processor of claim 6.

McGrath and Tran failed to teach wherein the instruction that permanently switches the decode logic from the first mode to the second mode succeeds a Java Impdep1 Bytecode.

However, Seal disclosed wherein the instruction that permanently switches the decode logic from the first mode to the second mode succeeds a Java Impdep1 Bytecode (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of McGrath and Tran.

New Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claim 34 is rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,973,562), in view of Tran (U.S. 6,367,006), further in view of Feierbach et al. (U.S. 6,088,786).

38. As per claim 34:

McGrath and Tran disclosed the processor of claim 21.

McGrath and Tran failed to teach wherein the decode logic is configured to decode instructions from the first instruction set being a stack-based instruction set, and is further configured to decode instructions from the second instruction set being a register-based instruction set.

However, Feierbach disclosed wherein the decode logic is configured to decode instructions from the first instruction set being a stack-based instruction set, and is further configured to decode instructions from the second instruction set being a register-based instruction set (Feierbach: Figure 2 element 227, column 7 lines 27-37)(Figure 2 shows a processor that is able to selectively execute stack-based instructions and register-based instructions by using a predecoder, element 227, to determine where the current instruction is to go. The combination with McGrath results in one of the ISA's being register-based and the other ISA being stack-based.).

The advantage of stack-based processors is that they are much more compact and efficient than there register-based counterparts. Having both a stack-based and register-based processor is advantageous when a processor also has to occasionally execute high-performance multimedia applications, which are better suited for register-based processors (Feierbach: Column 2 lines 44-67 continued to column 3 lines 1-45). One of ordinary skill in the art would have been motivated by the increased performance in certain applications for stack-based processors to add a stack-based processor to the processor of McGrath. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a stack-based processor alongside the register-based processor of McGrath for the advantage of increased performance in certain applications.

Response to Arguments

39. The arguments presented by Applicant in the response, received on 11/27/2007 are not considered persuasive.

40. Applicant argues "McGrath fails to teach or fairly suggest decoding instructions from the first instruction set in a first mode and decoding instructions from the second instruction set in a second mode" for claims 1, 9, 21, and 27.

This argument is not found to be persuasive for the following reason. The applicant also makes reference to Intel Software Developer's Manuals and states that a single instruction set spans 64, 32, and legacy 16 architectures. The examiner disagrees and states that legacy instruction sets cannot be reasonably interpreted as being lumped into a single ISA. Each transition from 8 bits, to 16 bits, to 32 bits, and now 64 bits usually brings with it new instructions that are to be executed within an ISA. An instruction set architecture as defined by the Microsoft computer dictionary fifth edition is the set of machine instructions that a processor recognizes and can execute. Today's processors have the burden of not only supporting their own instruction set architecture, but also those of past legacy processors. Thus, for example, an Intel processor executing instructions in 64-bit will also have to support past instruction set architectures of 32-bits, 16-bits, and 8 bits to ensure past programs written with these instruction sets are able to still execute. Therefore, the examiner is correct in his interpretation in that the 32-bit application and 64-bit operating system instructions each are separate ISA's.

41. Applicant argues "McGrath fails to teach or fairly suggest wherein the decoding of both instruction sets is performed on a single decoder" for claim 9.

This argument is not found to be persuasive for the following reason. The examiner stated that it's inherent that McGrath contains a decoder to decode the 32-bit application instructions and the 64-bit OS instructions. The decoding logic that decodes these instructions can be combined to be considered a single decoder. In addition, according to "In re Larson" (144 USPQ 347 (CCPA 1965)), to make integral doesn't give patentability over prior art.

42. Applicant argues "McGrath fails to teach or fairly a status register configured to indicate whether the decode logic is decoding instructions in the first mode or second mode" for claims 21 and 27.

This argument is not found to be persuasive for the following reason. The examiner stated that a plurality of status registers contain the bits that determine and specify the operating mode of the execution core. When this combined status register indicates the processor is executing 64-bit OS instructions, then the inherent decoder is inherently decoding the 64-bit OS instructions. The same also applies to the 32-bit application instructions.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

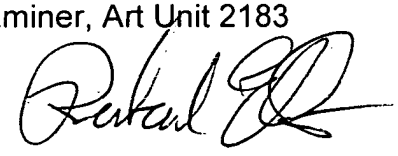
The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183



RICHARD L. ELLIS
PRIMARY EXAMINER